**What is Claimed is:**

1. A method of fabricating a Read Only Memory (ROM) device, comprising:

forming a first conductive layer pattern including a sidewall, on an insulating layer on an integrated circuit substrate;

implanting ions into the integrated circuit substrate using the first conductive layer pattern as an implantation mask;

thermally oxidizing at least a portion of the integrated circuit substrate and at least a portion of the sidewall to form a thermal oxide layer on at least the portion of the integrated circuit substrate and on the sidewall, and to form a buried doping layer from the implanted ions beneath the thermal oxide layer; and

forming a second conductive layer pattern on at least a portion of the thermal oxide layer and on at least a portion of the first conductive layer pattern.

2. A method according to Claim 1 wherein the first conductive layer pattern includes a bottom adjacent the integrated circuit substrate and a top opposite the integrated circuit substrate and wherein the thermally oxidizing comprises thermally oxidizing at least a portion of the integrated circuit substrate and at least a portion of the sidewall without thermally oxidizing the top and the bottom.

3. A method according to Claim 1 wherein the first conductive layer pattern comprises a first conductive layer on the insulating layer and a capping layer on the first conductive layer and wherein the following is performed between the thermally oxidizing and the forming a second conductive layer pattern:

removing the capping layer.

4. A method according to Claim 3 wherein the forming a first conductive layer pattern on an insulating layer on an integrated circuit substrate comprises:

forming an insulating layer on the integrated circuit substrate;

forming the first conductive layer on the insulating layer;

forming the capping layer on the first conductive layer;

forming a photoresist pattern on the capping layer; and

etching the capping layer and the first conductive layer using the photoresist pattern as an etch mask.

5. A method according to Claim 4 wherein the etching is followed by removing the photoresist pattern.

6. A method according to Claim 4:

wherein the following is performed between the forming a capping layer and forming a photoresist pattern:

forming an antireflection layer on the capping layer;

wherein the forming a photoresist pattern comprises forming a photoresist pattern on the antireflection layer; and

wherein the etching is followed by removing the photoresist pattern and the antireflection layer.

7. A method according to Claim 6 wherein the antireflection layer comprises an organic antireflection layer.

8. A method according to Claim 1 wherein the first and second conductive layer patterns both comprise polysilicon.

9. A method according to Claim 3 wherein the capping layer comprises silicon nitride.

10. A method according to Claim 1 further comprising selectively programming the ROM.

11. A method according to Claim 10 wherein the selectively programming comprises selectively implanting ions into the substrate.

12. A method according to Claim 3 wherein the following is performed between the forming a first conductive layer pattern and the implanting ions:

forming a hard mask on the capping layer;

forming a photoresist pattern on the hard mask;

etching the hard mask using the photoresist pattern; and

etching the first conductive layer pattern using the hard mask.

13. A method according to Claim 1 wherein a sidewall spacer is not formed on the sidewall of the first conductive layer pattern between the forming a first conductive layer and the thermally oxidizing.

14. An integrated circuit substrate Read Only Memory (ROM) device, comprising:

an integrated circuit substrate;

an insulating layer on the integrated circuit substrate;

a first conductive layer pattern including a sidewall, on the insulating layer opposite the integrated circuit substrate;

a thermal oxide layer on the integrated circuit substrate and directly on the sidewall of the first conductive layer pattern;

a buried doping layer in the integrated circuit substrate beneath the thermal oxide layer; and

a second conductive layer pattern on at least a portion of the thermal oxide layer and on at least a portion of the first conductive layer pattern.

15. A ROM device according to Claim 14 wherein the second conductive layer pattern is directly on the first conductive layer pattern opposite the insulating layer.

16. A ROM device according to Claim 14 wherein the first and second conductive layer patterns both comprise polysilicon.

17. A ROM device according to Claim 14 further comprising a programming region in the integrated circuit substrate.

18. A according to Claim 17 wherein the programming region comprises an implant region.

19. A ROM device according to Claim 14 wherein the second conductive layer pattern is not directly on the sidewall of the first conductive layer pattern.